Introduction :

Problem Specification :

Design a 4 bit ALU with three selection bits cs0, cs1 and cs2 for performing the following operations :

|  |  |  |  |
| --- | --- | --- | --- |
| Control Signals | | | Functions |
| Cs2 | Cs1 | Cs0 |
| 0 | 0 | 0 | AND |
| 0 | 0 | 1 | Sub |
| 0 | 1 | X | Decrement A |
| 1 | 0 | 0 | Complement A |
| 1 | 0 | 1 | XOR |
| 1 | 1 | X | Add |

Diagram

Description automatically generated

Truth Table :

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Cs2 | Cs1 | Cs0 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Table 2 : Arithmetic 4x1 MUX

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | Y\_i | S1 | S0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | X | X |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | B’\_i | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | X | X | X |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | X | X | X |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | B\_i | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | B\_i | 1 | 1 |

S\_0 = D1

S1 = D6⊕D7

Table 3: Logical 2x1 MUX

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | Y\_i | S |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | X | X |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | X | X |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | X | X |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | B\_i | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | X | X |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | X | X |

Y\_i = D5+ B\_i

S = D0

Table 4 : Combined Output

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | S |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

S = D0D4D5

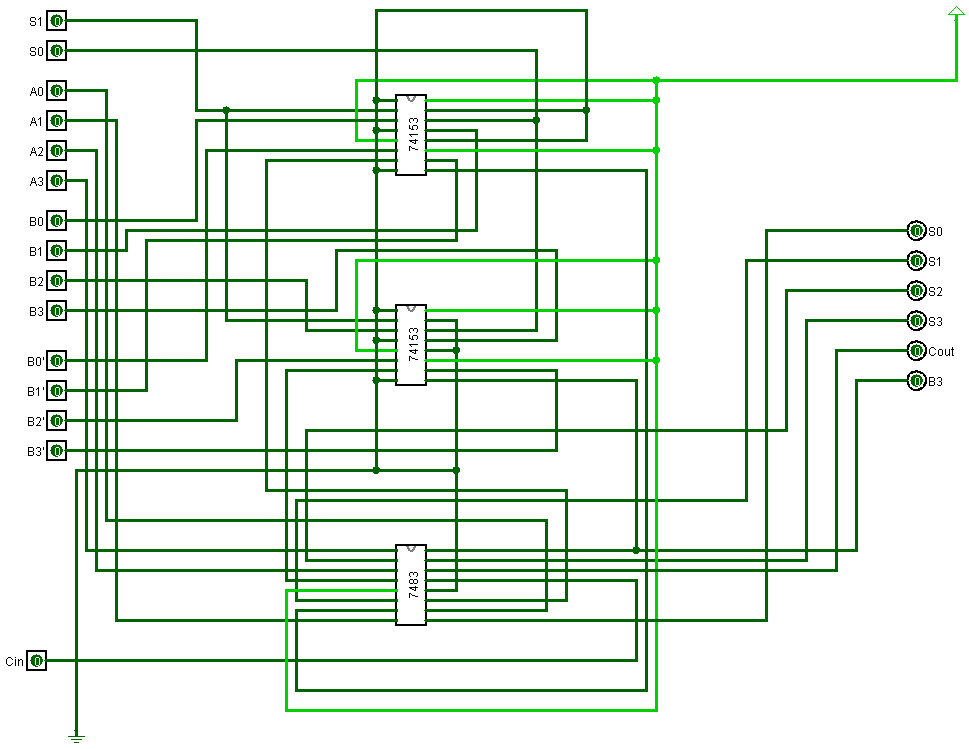
**Detailed Steps with necessary K-maps :**

**Block Diagram :**

**Diagram, schematic

Description automatically generated**

**Complete Circuit Diagram :**

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**Figure – 1: Arithmetic Unit**

**Diagram, schematic

Description automatically generated**

**Figure – 2: Logical Unit**

**Diagram, schematic

Description automatically generated**

**Figure – 3: Main unit**

**Required ICs** :

|  |  |
| --- | --- |
| **IC Name** | **Count** |
| IC 74138 (3 by 8 decoder) | 1 |
| IC 7483 (4 bit full adder) | 1 |
| IC 74157 (2 by 1 MUX) | 2 |
| IC 74153 (4 by 1 MUX) | 2 |
| IC 7408 (AND) | 2 |
| IC 7486 (XOR) | 2 |
| IC 7432 (OR) | 2 |
| IC 7404 (NOT) | 1 |

**Simulator Used : Logisim version 2.7.1**

**Discussion** :